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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/928,011	SEDLAK ET AL.	
	Examiner	Art Unit	
	Kevin P Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 have been examined.

2. Acknowledgement of the following papers filed: Amendment as received on 11/29/2004. The papers filed have been placed on record.

Withdrawn Objections

3. Applicant, via amendment, has overcome the objections to the drawings and title set forth in the previous Office Action. Consequently, these objections have been withdrawn by the examiner.

Withdrawn Rejections

4. Applicant, via amendment, has overcome the rejection under U.S.C. 112, second paragraph set forth in the previous Office Action. Consequently, this rejection has been withdrawn by the examiner.

5. Applicant, via persuasive arguments, has overcome the rejection under U.S.C. 102 and 103 of claims 1-7.

New Claim Rejections - 35 USC § 112

6. Claims 6 and 7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Multiple program counters each

having the capability to selectively add or subtract an instruction length or to not add or subtract an instruction length to the program counter is not disclosed. Also, multiple program counters being used with the selective adding or subtracting of an instruction length to an offset was not disclosed. It appears applicant combined two or three different embodiments, one with multiple program counters and one with selectively adding/subtracting an instruction length to a program counter and one with selectively adding/subtracting an instruction length to an offset value. However, this was not disclosed in the specification.

7. Claims 6 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim 6, "leaving the program counter" is claimed, when there was "a plurality of program counters," "one of the program counters" and "a program counter" previously mentioned. It is unclear which "program counter reading is unchanged" since there is no teaching of multiple program counters selectively having an instruction length added/subtracted to them in the specification.

New Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 2 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hauris, U.S. Patent 7,821,183 in view of Blomgren, U.S. Patent 5,781,750

10. As per claim 1, Hauris discloses a microprocessor for processing various assembler codes comprising:

-A plurality of program counters: (Abstract, Column 3, lines 34-35; Column 4, lines 16-41; Figure 2, items 22 and 30)

-A parameter designating a "program counter" (Column 4, lines 16-41, The output from flip flop 46, figure 2 designates a program counter)

-Depending on how the parameter is set, a different relative addressing takes place (Column 4, lines 16-41, The program counters hold different values to access different locations in memory, these values are then incremented when the selected program counter is active. Relative addressing is defined as, "An addressing mode in which the effective address is formed by adding an offset to the program counter (or a portion thereof) during execution." (The Authoritative Dictionary of IEEE Standards Terms) Therefore, incrementing a program counter is relative addressing, because the program counter has a current value, and a new value is reached by adding an offset to the current PC address.

-Dependent on the parameter, one of said program counters is active in a computation of relative addresses: (Column 4, lines 16-41, The output from flip flop 46, figure 2 designates a program counter)

11. While Hauris does teach a parameter selecting between program counters to access subroutines of instructions, he fails to teach wherein the subroutines are multiple assembler codes.

12. Blomgren teaches:

-Multiple assembler codes being processed: (x86 instruction set and PowerPC instruction set): Blomgren teaches that when a complex x86 instruction is reached, a new instruction pointer is loaded to indicate a software subroutine made up of PowerPC instructions.

13. It would have been obvious to one of ordinary skill in the art to combine the invention of Hauris with the multiple assembly codes of Blomgren because as Blomgren states, "Since there is so much installed x86 code, it is greatly desired to run x86 programs on newer RISC CPU's, without the performance degradation of a software emulator," column 3, lines 35-38. Blomgren does this by using a RISC and a CISC decoder, however, for the more complex x86 instructions, he uses a different instruction pointer to access a subroutine of RISC instructions in a ROM. Hauris already teaches accessing a ROM for a subroutine using multiple program counters. It would have been obvious to have the processor decode and execute both RISC and CISC instructions as taught in Blomgren by having decoders for both instruction sets, and using the ROM subroutine accessing method of Hauris to process the more complex CISC instructions.

This would cause said parameter of Hauris to indicate to switch assembly codes because the processor would be in a CISC mode until reaching a complex CISC instruction, at which point a RISC subroutine would be accessed via another program counter.

14. As per claim 2, Hauris, in view of Blomgren, disclose a microprocessor comprising:

-A computation unit: (Hauris, Figure 2 and column 3, lines 20-23, ROM/PLA 16 takes inputs and computes an output for CSDR 24)

-A multiplexer connected to said program counters (Hauris, Figure 2, item 32):

-Said multiplexer receives and is controlled by the parameter: (Hauris, Figure 2 shows the parameter as the input to items 22 and 30 into the CNT input and to the multiplexer input 2, the operation of the parameter is disclosed in column 4, lines 5-41; It is stated that the parameter turns on one program counter and turns off another when it designates a "subroutine call" or "subroutine return" instruction. CNT is part of the decoded parameter.

-Said multiplexer having an output connected to said computation unit for the relative addresses (Hauris, Figure 2, MUX 32 is directly connected to ROM/PLA 16, which is for the relative addresses)

15. As per claim 5, the hardware taught in regards to claim 1 implements the method of claim 5 and therefore, claim 5 is rejected for the same reasons set forth in regards to claim 1 above.

16. As per claim 6, Hauris, in view of Blomgren, teaches claim 5 as shown above, and further discloses:

-Performing one of an addition and a subtraction of an instruction length to/from a program counter reading for a relative address computation in dependence on one of the various operating states and the assembler codes: (Hauris, column 3, lines 31-40 and column 4, lines 16-41 and Abstract)

-Leaving the program counter reading unchanged: (Hauris, column 3, lines 31-40 and column 4, lines 16-41 and Abstract, When a program counter is not selected it remains unchanged. Also, between clock cycles a selected program counter's reading remains unchanged, because the program counter increments periodically, therefore there are periods when the program counter is constant and not incrementing.

17. As per claim 7, Hauris, in view of Blomgren, teaches claim 6 as shown above, and further discloses:

-Performing one of an addition and a subtraction of the instruction length to/from an offset value used for the computation of the relative addresses in dependence on one of the various operating states and the assembler codes: (Hauris, column 3, lines 31-40 and column 4, lines 16-41 and Abstract; The

values stored in the program counters are offsets, and are used for computation of relative addresses.)

-Leaving the offset value unchanged: (Hauris, column 3, lines 31-40 and column 4, lines 16-41 and Abstract; When a program counter is not selected, it's value (the offset) remains unchanged. Also, between clock cycles a selected program counter's reading remains unchanged because the program counter increments periodically, therefore, there are periods when the program counter is constant and not incrementing.)

18. Examiner also notes that as per claims 6 and 7, applicant claims, "performing one of:" and then lists two options multiple times. Therefore, only one of the two options must be met for a reference to teach the claims' limitations.

19. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goetz, U.S. Patent 5,854,913 in view of Yoshida, U.S. Patent 5,088,030, Baror, U.S. Patent 4,926,323, The PowerPC Architecture, 1994 and K. Short, Embedded Microprocessor Systems Design, 1998.

20. As per claim 3, Goetz discloses:

- A microprocessor for processing various assembler codes: (Abstract, line 1)

- Depending on how the parameter is set, a different relative addressing takes place: (Relative addressing is defined as, "An addressing mode in which the effective address is formed by adding an offset to the program counter (or a portion thereof) during execution." (The Authoritative

Dictionary of IEEE Standards Terms) Therefore, incrementing a program counter is relative addressing, because the program counter has a current value, and a new value is reached by adding an instruction length to the current PC address. Since the Q-bit indicates different instruction lengths to be added to the current PC address, different relative addressing takes place dependent on the Q-bit (Figure 9, Column 16, lines 47-64). Column

- A program counter (NIFA Compute 807, figure 9 and column 16, lines 47-64)

- A computation unit for computing relative addresses: (NIFA Compute 807, figure 9 and column16, lines 47-64)

21. While Goetz does teach multiple instruction sets being implemented and indicated by a parameter, Goetz is silent on how the different offsets for branch instructions are handled. It is well known in the art that PowerPC branch instructions add an offset to the address of the branch instruction (Page 36, numeral 1, The PowerPC Architecture), while x86 branch instructions add an offset to the address of the instruction following the branch instruction (Short, Embedded Microprocessor Systems Design, page 190, 2nd paragraph). However, since Goetz is silent on how the above issue is resolved, Goetz fails to teach:

- A multiplexer having a first input a second input for receiving a zero value, a third input receiving a parameter designating a respective assembler code, a memory for storing an instruction length having an output connected to said first input of said multiplexer

- An addition unit connected between said program counter and said computation unit, said adding unit having a first input connected to said program counter, a second input for an instruction length, and an output connected to said computation unit:

22. Yoshida teaches hardware to implement an x86-like branch instruction, which adds an offset to the address of the instruction following the branch instruction:

- A program counter (register 13, figure 2; Column 4, lines 8-20)

- A computation unit for computing relative addresses: (2nd Adder 17, figure 2 and column 4, lines 1-20)

- An addition unit connected between said program counter and said computation unit: (1st Adder 15)

-Said adding unit having a first input connected to said program counter, a second input for an instruction length, and an output connected to said computation unit: (Figure 2, the 1st adder 15 has the program counter (register 13) as an input, has an input for an instruction length ("Word Length"), and has an output connected to said computation unit (2nd Adder 17).

Yoshida teaches that the branch offset is calculated by adding an offset to the address of the instruction following the branch instruction. This occurs by adding a "Word Length" that is part of the instruction decoded (Figure 2 and column 4, lines 1-20)

23. It would have been obvious to add the hardware of Yoshida to implement the branch target address computation because hardware is inherently necessary in order to carry out the x86 relative branch instructions and because the invention of Yoshida eliminates time required by conventional processors to do branch target calculations (Abstract).

24. While Goetz, in view of Yoshida, teaches a method for handling the x86 branch instruction, it is still necessary to have hardware to implement the PowerPC branch instruction. One of ordinary skill in the art would have recognized that since the purpose of the 1st adder of Yoshida is to add the length of the branch instruction in order to complete the branch instruction that adds an offset to the address of the instruction following the branch instruction, it would have been obvious to simply add a zero as said "Word Length" offset to calculate a PowerPC branch target address. However, Goetz in view of Yoshida fails to teach that the "Word Length" values are stored in a memory and selected via a multiplexer with said parameter as an input.

25. Baror teaches hardwired values, an instruction length and a zero, as an input to an adder to be added to a program counter. Figure 7 shows the multiplexers 712, 716 and 719, which are used to select the offset to be added to the PC value selected from MUX 703. The PC value has one instruction length, a constant value inherently stored in memory, added to it (Column 17, lines 5-15) or can have a zero added to it (Column 17, line 36), see also Column 16, lines 25-28.

26. It would have been obvious to use a multiplexer to select a zero or an instruction length stored in a memory, and to select between the two for adding to the program counter to calculate a target branch address. One of ordinary skill in the art would have recognized that storing the instruction length ("Word Length") in the branch instruction takes up valuable instruction bits and increases the size of instructions and therefore the program size as well. It would have been obvious to use a multiplexer as taught in Baror, to reduce program size or to provide extra bits with which to encode other data or commands.

27. Since Goetz already teaches a parameter indicating which instruction set's offset to add to the program counter for sequential instruction fetching, one of ordinary skill in the art would have recognized to use the same parameter to indicate which offset to add for different non-sequential instruction fetching, i.e., the branch instructions of each instruction set, in order to avoid redundant hardware.

28. As per claim 4, Goetz, in view of Yoshida and Borar fail to teach the only limitation different from claim 3, which is "a subtracting unit" instead of an "adding unit."

29. However, Examiner takes Official Notice that numbers, including offsets, are very frequently represented in two's complement form, which allows simplified binary arithmetic operations.

30. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the offsets represented in two's complement form

since Examiner takes Official Notice two's complement form allows simplified binary arithmetic operations.

31. It is inherent that a binary adder is also a subtraction unit if the binary inputs are in two's complement form, because there is no difference in hardware between adding two's complement numbers and subtracting two's complement numbers. A two's complement adder is inherently a subtraction unit as well.

Response to Arguments

32. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

33. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4174. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KPR

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